Hahn Loeser • Parks

FAX TRANSMISSION

13 Rec'd PCT/PTO 06 MAR 2002

09/857859

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FROM:	Stephen L. Grant	Number of Pages: (including this pages)	22
DATE:	3/6/02	Client Code:	
SUBJECT:	Ser. No. 09/857,859	SEND BY:	Stephen L. Grant
TO:	Winston Alvarado	Facsimile Number:	703-305-3230

SENDER'S COMMENTS:

Mr. Alvarado:

I attach a copy of the papers mailed to the Patent Office on 13 September 2001 in this case. At the top of the papers attached is a photocopy of the return card we received from the Patent Office acknowledging receipt, dated 17 September 2001.

As noted in my comments in the paper filed in September, the decrease in the number of claims occurred as a result of amendment made during the PCT proceeding.

Please call me if you have any questions on this, at 330-864-5550.

Respectfully submitted,

Stephen L. Grant

Reg. No. 33390

Please note that the papers filed refer to 09/857,859 not 09/857,859 !!

SLG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Heinemann, et al	**Examiner:**	Alvarado, Winston
Serial No.:	09/857,857	**Group:**	PCT
Filed:	11 June 2001	**Date:**	12 September 2001

For: **BIPOLAR TRANSISTOR AND METHOD FOR PRODUCING SAME**

BOX PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

Enclosed please find the following:

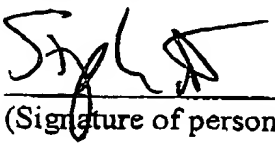
1. Response to Notice of Defective Response
2. Copy of Notification of a Defective Response
3. Acknowledgement of Return/Receipt Card

CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Date: 13 Sept. 2001

Stephen L. Grant
(Type or print name of person mailing paper)



(Signature of person mailing paper)

Attorney Docket No. 7 10-30 Initials SLC/bac Date

Inventor/Applicant Heinonen et al Ser./Pat. No. 09/852,857

Title Liquid Transfer Device Filed

☐ PATENT/DESIGN APPLICATION

_____ pgs. Specification

_____ pgs. Claims

_____ Total _____ Independent

_____ pgs. Abstract

_____ Sheet(s) of Drawings

_____ Formal _____ Informal

_____ Declaration/Power of Attorney

_____ Small Entity Status

_____ Certified Copy of Priority Document(s)

_____ PCT Request

_____ Fee Calculation Sheet

_____ Demand for Prel. Examination

_____ Base Issue Fee

_____ Supplemental Declaration

☑ AMENDMENT (Due 10/5/01)

_____ Extension of Time For _____ Month(s)

☐ INFORMATION DISCLOSURE STATEMENT

_____ PTO/SB/08A _____ Refs.

☐ ASSIGNMENT _____ Recordation

☐ CHECK(s) in Amount $ _____

☐ TRANSMITTAL _____ New Application

☑ OTHER Response to Restriction Requirement

Please Acknowledge

533 Rec'd PCT/PTO 17 SEP 2001

RECEIPT IS HEREBY ACKNOWLEDGED

Attorney's Docket 7040-30

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Heinemann, et al.	Examiner:	Alvarado, Winston
Ser. No.:	09/857,857	Art Group:	PCT
Title:	BIPOLAR TRANSISTOR AND METHOD FOR PRODUCING SAME		
Filed:	11 June 2001	Date:	12 September 2001

RESPONSE TO NOTICE OF DEFECTIVE RESPONSE

This response is made to the Notification of Defective Response mailed 5 September 2001 in the above matter. As this response is filed within thirty days after the mailing date, this response is made with no extension fee believed to be due. If any extension fee is due, please charge it to Deposit Account 15-0450.

REMARKS

The translation of the application as filed on 23 August 2001 was the translation of the application as amended in the PCT proceeding on 15 November 2000. As a result of that amendment, only 11 claims were left in the case, and those are the claims which have been amended in the preliminary amendment filed on 23 August 2001.

The undersigned attaches two documents with this response. The first of these is the literal translation of the case as initially filed in the PCT on 8 December 1999. It is marked as SPEC AS INITIALLY FILED and contains 18 claims. The second document is a literal translation of the amended specification and claims that were filed in the EPO on 15 November 2000. The second document is marked as SPEC AS AMENDED IN PCT and contains 11 claims.

Respectfully submitted,

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U.S. APPLICATION NO.		FIRST NAMED APPLICANT	ATTY. DOCKET NO.
09/857859		HEINEMANN B	7040-30

INTERNATIONAL APPLICATION NO.
PCT/DE99/03961

I.A. FILING DATE	PRIORITY DATE
08 DEC 99	14 DEC 98

OLDHAM & OLDHAM CO.
TWIN OAKS ESTATE
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DATE MAILED: 05 SEP 2001

NOTIFICATION OF A DEFECTIVE RESPONSE

1. ☐ The request for an extension of time (37 CFR 1.136(a)) filed _____ is defective because the required fee is missing/insufficient. Extension of time fees are listed at 37 CFR 1.17(a)(1)-(a)(5).

2. ☐ Applicant's response filed _____ was received in the Office after the expiration of the period for response set in the Office notification mailed _____. This application will become abandoned unless applicant obtains an extension of time to reply to the last Office notification under 37 CFR 1.136(a).

3. ☑ Applicant's response filed 23 AUGUST 2001 is hereby acknowledged. The following requirements set forth in the NOTIFICATION of MISSING REQUIREMENTS (Form PCT/DO/EO/905) mailed 31 JUL 2001 have not been completed.

- ☑ Translation of the international application into English.
  - ☑ which is defective for the reasons indicated on the attached Notice of Defective Translation.
- ☐ Processing fee (37 CFR 1.492(f)).
- ☐ Oath or Declaration of inventor(s).
  - ☐ not in compliance with 37 CFR 1.497(a) and (b) for the reasons indicated on the attached PCT/DO/EO/917.
- ☐ Surcharge (37 CFR 1.492(e)).
- ☐ Sequence Listing.
  - ☐ not in compliance with 37 CFR 1.821-1.825 for the reasons indicated on the attached PCT/DO/EO/920.
- ☐ Additional claim fees.

Applicant is required to complete the response within a time limit of ONE MONTH from the date of this Notification or within the time remaining in the response set forth in the Notification of Missing Requirements (Form DO/EO/905), whichever is the longer. No extension of this time limit may be granted under 37 C.F.R. § 1.136, but the period for response set in the Notification of Missing Requirements (Form DO/EO/905) may be extended under 37 C.F.R. § 1.136(a).

Applicant is reminded that any communication to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
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U.S. APPLICATION NO.	ATTACHMENT TO FORM PCT/DO/EO/
09/857859	

NOTICE OF DEFECTIVE TRANSLATION

The received translation is defective because:

☐ (1) The text in the drawings has not been properly translated;

■ (2) The number of claims in the International Application and the number of claims in the translation are not the same;

☐ (3) The translation of the International Application is incomplete as a number of pages are missing;

☐ (4) Other.

Please submit a translated copy of the international application as filed with the eighteen claims to enable me to complete processing this application

Winston M. Alvarado

Telephone: 703-305-6421

Bi-polar transistor and a procedure for its manufacture

The invention relates to a bi-polar transistor and a procedure for its manufacture.

The implementation of epitaxially manufactured silicon-germanium hetero-bi-polar transistors (SiGe HBT) and the [resulting] cost-reducing simplification of the technological processes have lately provided a new impetus for a further development of Si bi-polar transistors. In this respect, the combination of an epitaxially produced base with the process-simplifying possibilities of the single polysilicon technology offers an attractive direction of development.

In comparison with conventional base profiles produced by implantation or diffusion, silicon-germanium base layers made by epitaxy allow producing, simultaneously, smaller base widths and base layer resistance without unusable small current gains or high leakage currents. The technology allows implementation of a concentration of the active doping agent of up to 1 x 10^{20} cm^{-3}, as is described – for example – in *A. Schüppen, A. Gruhle, U. Erben, H. Kibbel und U. König: 90 GHz fmax SiGe-HBTs, DRC 94*, page IIA-2, 1994. However, in order to prevent leakage currents due to tunnel processes, a low-doped region is required between the high-concentration zones of the emitter and the base. As a matter of fact, if the base doping exceeds the value of 5 x 10^{18} cm^{-3}, and if the high concentration of the emitter reaches down to the base – as is usual with implanted base profiles – the consequence is the existence of unacceptably high tunnel currents. As opposed to implanted base profiles, the application of epitaxy allows, simultaneously and without any problems, the production of narrow base profiles and a low-doped region (cap layer).

Figure 1 illustrates the emitter zone of a SiGe HBT. This transistor design reflects typical characteristics of a single poly-silicon process. An SiGe base 12 and subsequently a cap layer 13 were deposited over a monocrystal collector zone 11. Figure 1 does not show a lateral insulation of the transistor zone. If semiconductor material grows both on the monocrystal substrate 11 and on the insulator zone – not shown in the picture – (i.e., differential epitaxy), it is possible to utilize the grown semiconductor layers as a connection between a contact on the insulation zone and the inner transistor. Such a connection should be designed with as low impedance as possible. This is why it would be advantageous if the epitaxial layer thickness could be set up independently from the base width. A poly-silicon or an α-silicon layer 15 is deposited on an insulation layer 14, in which emitter windows were etched by means of a wet-chemical etching process. During the deposition or subsequently, the α-silicon layer 15 obtains – by implantation – a doping of the emitter's conductivity type and serves as diffusion source for the emitter doping 16 in the monocrystal substrate. Insulator layer 14 is applied in order to prevent damage to cap layer 13 during the structuring of the polycrystal α-silicon layer 15 performed later. In the overlapping region 17 – a zone between the edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer 15, a layer sequence arises consisting of semiconductor material, insulator material and semiconductor material. Depending on the doping of the cap layer 13, the interfacial charges and the recombination properties of the surface as well as on the operation conditions of the transistor, this design can cause – analogous to a MOS capacity – an enhancement but also a depletion of mobile charge carriers on the

surface of the cap layer 13. With a forward-current base-emitter diode, this can affect both the ideal nature of the base current and the low-frequency noise properties. Under certain circumstances, generation currents and breakdown voltage in the non-conducting direction can be affected. The condition that – due to the tunnel [currents] danger – the doping agent concentration should not exceed the value of 5×10^{18} cm^{-3} leads to the question, by means of which procedure this zone should be suitably doped. The following text discusses the variants for SiGe HBT so far known: homogeneous n-doping or p-doping near the tunnel limit or quasi undoped zones (i-zones). *A. Chantre, M. Marty, J.L. Regolini, M. Mouis, J. de Pontcharra, D. Dutrtre, C. Morin, D. Gloria, S. Jouan, R. Pantel, M. Laurens and A. Monroy: A high performance low complexity SiGe HBT for BiCMOS integration, BCTM '98, 1998*, pages 93 – 96 uses a p-doping of about 5×10^{18} cm^{-3}. This results in a decisive disadvantage in that the thickness of the cap layer must be set up within a tolerance range of a few nanometers from the penetration depth of the doping agent diffusing from the poly-silicon emitter layer. Greater cap layer thickness values (which would be advantageous for a low-impedance connection between the inner base and a connector in the insulation zone) are not possible since it would negatively affect the effect of the germanium profile. *A. Gruhle, C. Mähner: Low l/f noise SiGe HBTs with application to low phase noise microwave oscillators, Electronics Letters, Vol. 33, No. 24, 1997*, pages 2050 – 2052 uses a cap layer 100 nm thick with an n-concentration of $1 - 2 \times 10^{18}$ cm^{-3}. Although this variant eliminates the problem of the thickness tolerance, and avoids the danger of tunnel currents by reducing the doping agent concentration in the cap layer, it still does not take full advantage of the possibilities of reducing the base-emitter capacity.

This disadvantage can be eliminated by not doping the cap layer as is described, for example, in *B. Heinemann, F. Herzel and U. Zillmann: Influence of low doped emitter and collector regions on high-frequency performance SiGe-base HBTs, Solid-St. Electron, 1995*, Volume 38(6), pages 1183 - 1189. However, it can easily lead to a depletion of the aforementioned overlapping region 17. These connections are explained in further text by means of a two-dimension design element simulation.

Figure 2 shows the simplified transistor design used in the simulation. The electrical effect of the oxide semiconductor surface in the overlapping region is modeled by means of a positive surface charge density of 1×10^{11} cm^{-2} and a surface recombination speed of 1000 cm/s. Figure 3 illustrates vertical profiles along a section line horizontal to the overlapping region. The profiles show three doping variants in the cap layer 13 and a p-doped SiGe base 12 identical for all three cases. The following cap doping cases are compared: a quasi undoped cap layer 13 (profile i) and two homogeneous n-dopings (profile n1 with 1×10^{18} cm^{-3} and profile n2 with 2×10^{17} cm^{-3}). Figure 4 shows the transition frequency as a function of the collector current for various doping variants. Especially with small collector currents, an increase in transition frequency with a falling doping level in the cap layer 13 can be noticed. While profile i provides relatively best transition frequencies, it has, however, the disadvantage that the ideal nature of the base current (Figure 5) is noticeably affected in comparison with the other profiles.

The task of this invention is to indicate a bi-polar transistor and a procedure for its manufacture that eliminates the described disadvantages of conventional arrangements, in order to achieve especially minimal base-emitter capacities and best high-frequency properties without noticeably affecting the static properties of the bi-polar transistor with a low-doped cap layer -

above all the ideal nature of the base current and low-frequency noise – and without increasing the process complexity.

This invention fulfills this task by introducing a special doping profile into an epitaxially produced cap layer (cap doping). This doping profile allows achieving a minimal base-emitter capacity and best high-frequency properties, but also restricts the effect of a generation-active and recombination-active interface between the cap layer and the insulator in the overlapping poly-silicon region in the interesting function range of the transistor, and improves the ideal nature of the base current.

Decisive for the good high-frequency properties is the base-side section in the cap layer of a preferable thickness between 20 nm and 70 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}.

On the emitter side, the cap layer is doped more highly. If the doping agent is of a conductivity type like the base layer, the doping agent concentration applied in the cap layer is preferably less than 5×10^{18} cm^{-3} in order to prevent tunnel currents.

The cap doping profile is preferably introduced by implantation in situ during the epitaxy procedure.

The characteristics of this invention are clear from the claims and also from the description and the drawings, where each characteristic – either individually or several characteristics in the form of sub-combinations – represent patentable designs, for which protection is demanded herein. Design examples are illustrated in the drawings and are explained in more detail in further text.

The drawings show:

Figure 1: A schematic illustration of the emitter zone of a bi-polar transistor manufactured with a single poly-silicon technology with an epitaxially deposited base,

Figure 2: A schematic illustration of the simulation region for the bi-polar transistor according to Fig. 1 (not in correct scale),

Figure 3: Vertical doping profiles under the overlapping region for various cap doping levels,

Figure 4: Transition frequency as a function of the collector current density for various doping profiles,

Figure 5: Graphs for various doping profiles,

Figure 6: Vertical doping profiles under the overlapping region for various cap doping levels,

Figure 7: Graphs for various doping profiles,

Figure 8: Transition frequency as a function of the collector current density for various doping profiles, and

Figure 9: A schematic illustration of a bi-polar transistor during the manufacturing process.

The characteristics and effects of the cap doping profiles according to this invention are described by means of a two-dimensional element simulation on an npn SiGe HBT. The explanation can be applied to a pnp transistor accordingly.

Figure 6 shows characteristic examples for the vertical profiles (as proposed herein) in the cap layer 13 along a section line horizontal to the overlapping region. The [doping agent concentration of the] cap "profile p1" is growing in direction to the surface of the cap layer and reaches there its maximum concentration with about 9×10^{17} cm^{-3}, whereas the box-like profiles "p2" and "n3" are 10 nm wide and doped with 2×10^{18} cm^{-3}. The profiles p1 p2 are of a p conductivity type, profile n3 is of n-type. Figure 7 shows "Gummel" graphs to profiles p1, p2 and n3, when the characteristics of profile 1 from Fig. 5 were taken over for comparison. Figure 7 shows a clear improvement in the characteristics of the base current when cap doping is used as compared with the behavior of profile i. Dynamic calculations to these profiles lead to the results shown in Figure 8: Unlike the homogeneous dopings n1 and n2 with concentrations of 1×10^{18} cm^{-3} and 2×10^{17} cm^{-3}, profiles p1, p2 and n3 demonstrate no noticeable deterioration of transition frequencies in comparison with profile i. Decisive for the good high-frequency properties is the section in the cap layer of a preferable thickness of at least 20 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}. The results indicate that, in the example shown here, n-profiles and n-profiles in the cap layer can achieve comparable results.

In practice, the decision which doping type should be applied depends on the circumstance, e.g., of which type and density are the charges on the Si/insulator interface or in the insulator, or which manufacturing procedure can be used for the cap doping process. So, e.g., the proposed profiles can be introduced by implantation. However, this variant should be preferred only if the effects of point defects on the base profile can be controlled. Should the curing of the point defects lead to an increased diffusion of the base doping from the SiGe layer and, therefore, to an unacceptable deterioration of the electrical properties, other doping variants are required. For example, an in situ doping during the epitaxy process is possible. During this procedure, the type of the cap doping is co-determined by the safety and simplicity of the deposition process. The following text explains the manufacturing of a bi-polar transistor according to this invention on the example of an npn SiGe HBT. The revealed procedure can be applied to pnp transistors as well. In addition, according to this invention it is also possible not to use an epitaxy process on the base layer and, instead, introduce the base profile by implantation before the epitaxial manufacturing of the cap layer.

As illustrated in Figure 9, structured regions consisting of a collector region 112 of the conductivity type II and an insulation region 113 (which surrounds the collector region 112) were produced on a monocrystal substrate layer 111 of the conductivity type I. If the emitter and

the collector are, e.g., n-conductive, the base is of the p-type and vice versa. Various suitable insulation techniques are known such as LOCOS processes, spaced mesa arrangements or deep or flat trench insulation.

On the basis of a differential epitaxy process, a buffer layer 114, a SiGe layer with in-situ doping of the base layer 115 of the conductivity type I and a cap layer 116 are is applied on the entire surface.

While the buffer layer 114, the base layer 115 and the cap layer 116 grow – as monocrystal materials – on the silicon substrate, polycrystal layers 114/1, 115/1 and 116/1 arise over the insulation zone 113. After photolithographic masking, dry-etching techniques are applied to remove the epitaxy layer in those regions in which no transistors arise.

If a selective epitaxy process is used instead of differential epitaxy, where growth occurs exclusively on the silicon underground, the structuring of the epitaxy layer stack is eliminated.

In the following step, the silicon regions with an insulation layer 117 are exposed. This can be achieved by means of thermal oxidation and/or deposition. Layer stacks of dielectrica such as silicon oxide and silicon nitride can be applied. Besides that, the electrically conductive layer can be covered with a poly-silicon layer in order to maintain additional flexibility for the process at a later stage.

Essential from the point of view of the procedure according to this invention is the implementation of the cap doping profile in an epitaxially produced cap layer. There is a possibility to introduce similar profiles, as shown in Figure 6, in situ during the epitaxy process. Furthermore, a flat profile can be produced by implantation before or after the production of the insulation layer 117. In addition, various procedures for the diffusion of such profiles are also known. This can also be performed by means of an insulation layer highly enriched with the doping agent. A diffusion step can occur before or after further procedure steps. The use of diffusion-preventing ingredients in the collector, the base and the cap layer 116 such as carbon is especially useful if certain processes are used such as implantation, diffusion or thermal oxidation, which can cause an accelerated diffusion of the doping agents.

The transistor manufacturing process can now proceed with the structuring of a coating mask for the opening of the emitter window. In this step, the cover layers are removed in well-known etching procedures. In order to achieve good transistor properties, preferably wet-etching techniques should be used to expose the semiconductor surface.

The process continues with the deposition of an amorphous silicon layer for the creation of a poly-silicon emitter. This layer can be doped in situ by implantation during or immediately after the deposition.

The process then continues with conventional steps of structuring, implantation and passivation. The required high-temperature steps are taken to cure implantation defects and to form the poly-emitter. The manufacturing process is completed with the opening of the contact

apertures for the emitter, the base and the collector and with a standard metallization of the transistor contacts.

This invention explains, on the basis of concrete design examples, a bi-polar transistor and a procedure for its manufacture. However, notice must be taken that this invention is not restricted to the particulars of the description of any particular design example, since, within the patent claims, changes and deviations are also subject to patent protection.

Patent claims

1. A procedure for the manufacture of a bi-polar transistor, during which structured regions consisting of a collector region (112) and an insulation region (113) - which surrounds the collector region (112) - are produced on a monocrystal substrate layer (111), a base layer (115) and, by means of epitaxy, a cap layer (116) are produced over the collector zone (112), an insulation layer (117) is deposited over the cap layer (116), the insulation layer (117) is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer (117) and is then used as an emitter-doping agent source and as a contact layer, **characterized in that** a doping profile is introduced into the cap layer (116), and the profile is low-doped on the base side and highly doped on the emitter side.

2. A procedure according to claim 1, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed values of 5×10^{16} cm^{-3}.

3. A procedure according to claims 1 or 2, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed the thickness of 70 nm.

4. A procedure according to one or several of the preceding claims, **characterized in that** the base-side lower doping concentration of the cap layer (116) of a layer thickness of 20 nm does not exceed values of 5×10^{16} cm^{-3}.

5. A procedure according to one or several of the preceding claims, **characterized in that** the emitter-side high doping concentration of the cap layer (116) does not exceed values of
5×10^{18} cm^{-3} if the doping agent is of the same conductivity type as the base layer (115).

6. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced by implantation.

7. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced in situ during the epitaxy process.

8. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced by diffusion from the insulation layer (117) that had been highly enriched with the doping agent.

9. A procedure according to one or several of the preceding claims, **characterized in that** the base is produced by epitaxy.

10. A procedure according to one or several of the preceding claims, **characterized in that** the base layer (115) is implemented as an SiGe layer by epitaxy.

11. A procedure according to one or several of the preceding claims, **characterized in that** a diffusion-preventing ingredient is introduced into the collector zone (112), the base layer (115) and/or the emitter zone.

12. A procedure according to one or several of the preceding claims, **characterized in that** carbon is introduced as a diffusion-preventing ingredient.

13. A procedure according to one or several of the preceding claims, **characterized in that** boron in a concentration of over 5×10^{18} cm^{-3} is introduced into the base layer (115).

14. A bi-polar transistor, in which structured regions consisting of a collector region (112) and an insulation region (113) - which surrounds the collector region (112) - are produced on a monocrystal substrate layer (111), a base layer (115) and, by means of epitaxy, a cap layer (116) are produced over the collector zone (112), an insulation layer (117) is deposited over the cap layer (116), the insulation layer (117) is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer (117) and is then used as an emitter-doping agent source and as a contact layer, **characterized in that** a doping profile is introduced into the cap layer (116), and the profile is low-doped on the base side and highly doped on the emitter side.

15. A bi-polar transistor according to claim 14, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed values of 5×10^{16} cm^{-3}.

16. A bi-polar transistor according to claims 14 or 15, **characterized in that** the base-side lower doping concentration of the cap layer (116) of a layer thickness of at least 20 nm does not exceed values of 5×10^{16} cm^{-3}.

17. A bi-polar transistor according to one or several of claims 14 to 16, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed the thickness of 70 nm.

18. A bi-polar transistor according to one or several of claims 14 to 17, **characterized in that** the emitter-side high doping concentration of the cap layer (116) does not exceed values of 5×10^{18} cm^{-3} if the doping agent is of the same conductivity type as the base layer (115).

Summary

The task of this invention is to indicate a bi-polar transistor and a procedure for its manufacture that achieves minimal base-emitter capacities and best high-frequency properties without noticeably affecting the static properties of the bi-polar transistor with a low-doped cap layer - above all the ideal nature of the base current and low-frequency noise – and without increasing the process complexity.

This invention fulfills this task by introducing a special doping profile into an epitaxially produced cap layer (cap doping). This doping profile allows achieving a minimal base-emitter capacity and best high-frequency properties, but also restricts the effect of a generation-active and recombination-active interface between the cap layer and the insulator in the overlapping poly-silicon region in the interesting function range of the transistor, and improves the ideal nature of the base current.

Decisive for the good high-frequency properties is the base-side section in the cap layer of a preferable thickness between 20 nm and 70 nm with low-concentration doping, preferably less then 5 x 10^{16} cm^{-3}.

Figures 1 to 9:

Polysilizium = poly-silicon
SiGe-Basis = SiGe base
Kollektor = collector
Cap-Schicht = cap layer
Konzentration = concentration
Profil = profile
Abstand zur Si/SiO_2 Grenzfläche = distance to Si/SiO_2 surface
Transitfrequenz = transition frequency
Kollektorstrom = collector current
Basis = base
Spannung = voltage

Bi-polar transistor and a procedure for its manufacture

The invention relates to a bi-polar transistor and a procedure for its manufacture.

The implementation of epitaxially manufactured silicon-germanium hetero-bi-polar transistors (SiGe HBT) and the [resulting] cost-reducing simplification of the technological processes have lately provided a new impetus for a further development of Si bi-polar transistors. In this respect, the combination of an epitaxially produced base with the process-simplifying possibilities of the single polysilicon technology offers an attractive direction of development.

In comparison with conventional base profiles produced by implantation or diffusion, silicon-germanium base layers made by epitaxy allow producing, simultaneously, smaller base widths and base layer resistance without unusable small current gains or high leakage currents. The technology allows implementation of a concentration of the active doping agent of up to 1 x 10^{20} cm^{-3}, as is described – for example – in *A. Schüppen, A. Gruhle, U. Erben, H. Kibbel und U. König: 90 GHz fmax SiGe-HBTs, DRC 94*, page IIA-2, 1994. However, in order to prevent leakage currents due to tunnel processes, a low-doped region is required between the high-concentration zones of the emitter and the base. As a matter of fact, if the base doping exceeds the value of 5 x 10^{18} cm^{-3}, and if the high concentration of the emitter reaches down to the base – as is usual with implanted base profiles – the consequence is the existence of unacceptably high tunnel currents. As opposed to implanted base profiles, the application of epitaxy allows, simultaneously and without any problems, the production of narrow base profiles and a low-doped region (cap layer).

Figure 1 illustrates the emitter zone of a SiGe HBT. This transistor design reflects typical characteristics of a single poly-silicon process. An SiGe base 12 and subsequently a cap layer 13 were deposited over a monocrystal collector zone 11. Figure 1 does not show a lateral insulation of the transistor zone. If semiconductor material grows both on the monocrystal substrate 11 and on the insulator zone – not shown in the picture – (i.e., differential epitaxy), it is possible to utilize the grown semiconductor layers as a connection between a contact on the insulation zone and the inner transistor. Such a connection should be designed with as low impedance as possible. This is why it would be advantageous if the epitaxial layer thickness could be set up independently from the base width. A poly-silicon or an α-silicon layer 15 is deposited on an insulation layer 14, in which emitter windows were etched by means of a wet-chemical etching process. During the deposition or subsequently, the α-silicon layer 15 obtains – by implantation – a doping of the emitter's conductivity type and serves as diffusion source for the emitter doping 16 in the monocrystal substrate. Insulator layer 14 is applied in order to prevent damage to cap layer 13 during the structuring of the polycrystal α-silicon layer 15 performed later. In the overlapping region 17 – a zone between the edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer 15, a layer sequence arises consisting of semiconductor material, insulator material and semiconductor material. Depending on the doping of the cap layer 13, the interfacial charges and the recombination properties of the surface as well as on the operation conditions of the transistor, this design can cause – analogous to a MOS capacity – an enhancement but also a depletion of mobile charge carriers on the

surface of the cap layer 13. With a forward-current base-emitter diode, this can affect both the ideal nature of the base current and the low-frequency noise properties. Under certain circumstances, generation currents and breakdown voltage in the non-conducting direction can be affected. The condition that – due to the tunnel [currents] danger – the doping agent concentration should not exceed the value of 5×10^{18} cm^{-3} leads to the question, by means of which procedure this zone should be suitably doped. The following text discusses the variants for SiGe HBT so far known: homogeneous n-doping or p-doping near the tunnel limit or quasi undoped zones (i-zones). *A. Chantre, M. Marty, J.L. Regolini, M. Mouis, J. de Pontcharra, D. Dutrtre, C. Morin, D. Gloria, S. Jouan, R. Pantel, M. Laurens and A. Monroy: A high performance low complexity SiGe HBT for BiCMOS integration, BCTM '98, 1998*, pages 93 – 96 uses a p-doping of about 5×10^{18} cm^{-3}. This results in a decisive disadvantage in that the thickness of the cap layer must be set up within a tolerance range of a few nanometers from the penetration depth of the doping agent diffusing from the poly-silicon emitter layer. Greater cap layer thickness values (which would be advantageous for a low-impedance connection between the inner base and a connector in the insulation zone) are not possible since it would negatively affect the effect of the germanium profile. *A. Gruhle, C. Mähner: Low l/f noise SiGe HBTs with application to low phase noise microwave oscillators, Electronics Letters, Vol. 33, No. 24, 1997*, pages 2050 – 2052 uses a cap layer 100 nm thick with an n-concentration of $1 - 2 \times 10^{18}$ cm^{-3}. EP-A-0 795 899 indicates similar conditions, where preferably a cap layer of a thickness of 70 nm with a n-doping concentration of 2×10^{18} cm^{-3} is used. Although this variant eliminates the problem of the thickness tolerance, and avoids the danger of tunnel currents by reducing the doping agent concentration in the cap layer, it still does not take full advantage of the possibilities of reducing the base-emitter capacity.

This disadvantage can be eliminated by not doping the cap layer as is described, for example, in *B. Heinemann, F. Herzel and U. Zillmann: Influence of low doped emitter and collector regions on high-frequency performance SiGe-base HBTs, Solid-St. Electron, 1995*, Volume 38(6), pages 1183 - 1189. However, it can easily lead to a depletion of the aforementioned overlapping region 17. These connections are explained in further text by means of a two-dimension design element simulation.

Figure 2 shows the simplified transistor design used in the simulation. The electrical effect of the oxide semiconductor surface in the overlapping region is modeled by means of a positive surface charge density of 1×10^{11} cm^{-2} and a surface recombination speed of 1000 cm/s. Figure 3 illustrates vertical profiles along a section line horizontal to the overlapping region. The profiles show three doping variants in the cap layer 13 and a p-doped SiGe base 12 identical for all three cases. The following cap doping cases are compared: a quasi undoped cap layer 13 (profile i) and two homogeneous n-dopings (profile n1 with 1×10^{18} cm^{-3} and profile n2 with 2×10^{17} cm^{-3}). Figure 4 shows the transition frequency as a function of the collector current for various doping variants. Especially with small collector currents, an increase in transition frequency with a falling doping level in the cap layer 13 can be noticed. While profile i provides relatively best transition frequencies, it has, however, the disadvantage that the ideal nature of the base current (Figure 5) is noticeably affected in comparison with the other profiles.

The task of this invention is to indicate a bi-polar transistor and a procedure for its manufacture that eliminates the described disadvantages of conventional arrangements, in order

to achieve especially minimal base-emitter capacities and best high-frequency properties without noticeably affecting the static properties of the bi-polar transistor with a low-doped cap layer - above all the ideal nature of the base current and low-frequency noise – and without increasing the process complexity.

This invention fulfills this task by introducing a special doping profile into an epitaxially produced cap layer (cap doping). This doping profile allows achieving a minimal base-emitter capacity and best high-frequency properties, but also restricts the effect of a generation-active and recombination-active interface between the cap layer and the insulator in the overlapping poly-silicon region in the interesting function range of the transistor, and improves the ideal nature of the base current.

Decisive for the good high-frequency properties is the base-side section in the cap layer of a preferable thickness between 20 nm and 70 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}.

On the emitter side, the cap layer is doped more highly. If the doping agent is of a conductivity type like the base layer, the doping agent concentration applied in the cap layer is preferably less than 5×10^{18} cm^{-3} in order to prevent tunnel currents.

The cap doping profile is preferably introduced by implantation in situ during the epitaxy procedure.

The characteristics of this invention are clear from the claims and also from the description and the drawings, where each characteristic – either individually or several characteristics in the form of sub-combinations – represent patentable designs, for which protection is demanded herein. Design examples are illustrated in the drawings and are explained in more detail in further text.

The drawings show:

Figure 1: A schematic illustration of the emitter zone of a bi-polar transistor manufactured with a single poly-silicon technology with an epitaxially deposited base,

Figure 2: A schematic illustration of the simulation region for the bi-polar transistor according to Fig. 1 (not in correct scale),

Figure 3: Vertical doping profiles under the overlapping region for various cap doping levels,

Figure 4: Transition frequency as a function of the collector current density for various doping profiles,

Figure 5: Graphs for various doping profiles,

Figure 6: Vertical doping profiles under the overlapping region for various cap doping

levels,

Figure 7: Graphs for various doping profiles,

Figure 8: Transition frequency as a function of the collector current density for various doping profiles, and

Figure 9: A schematic illustration of a bi-polar transistor during the manufacturing process.

The characteristics and effects of the cap doping profiles according to this invention are described by means of a two-dimensional element simulation on an npn SiGe HBT. The explanation can be applied to a pnp transistor accordingly.

Figure 6 shows characteristic examples for the vertical profiles (as proposed herein) in the cap layer 13 along a section line horizontal to the overlapping region. The [doping agent concentration of the] cap "profile p1" is growing in direction to the surface of the cap layer and reaches there its maximum concentration with about 9×10^{17} cm^{-3}, whereas the box-like profiles "p2" and "n3" are 10 nm wide and doped with 2×10^{18} cm^{-3}. The profiles p1 p2 are of a p conductivity type, profile n3 is of n-type. Figure 7 shows "Gummel" graphs to profiles p1, p2 and n3, when the characteristics of profile 1 from Fig. 5 were taken over for comparison. Figure 7 shows a clear improvement in the characteristics of the base current when cap doping is used as compared with the behavior of profile i. Dynamic calculations to these profiles lead to the results shown in Figure 8: Unlike the homogeneous dopings n1 and n2 with concentrations of 1×10^{18} cm^{-3} and 2×10^{17} cm^{-3}, profiles p1, p2 and n3 demonstrate no noticeable deterioration of transition frequencies in comparison with profile i. Decisive for the good high-frequency properties is the section in the cap layer of a preferable thickness of at least 20 nm with low-concentration doping, preferably less then 5×10^{16} cm^{-3}. The results indicate that, in the example shown here, n-profiles and n-profiles in the cap layer can achieve comparable results.

In practice, the decision which doping type should be applied depends on the circumstance, e.g., of which type and density are the charges on the Si/insulator interface or in the insulator, or which manufacturing procedure can be used for the cap doping process. So, e.g., the proposed profiles can be introduced by implantation. However, this variant should be preferred only if the effects of point defects on the base profile can be controlled. Should the curing of the point defects lead to an increased diffusion of the base doping from the SiGe layer and, therefore, to an unacceptable deterioration of the electrical properties, other doping variants are required. For example, an in situ doping during the epitaxy process is possible. During this procedure, the type of the cap doping is co-determined by the safety and simplicity of the deposition process. The following text explains the manufacturing of a bi-polar transistor according to this invention on the example of an npn SiGe HBT. The revealed procedure can be applied to pnp transistors as well. In addition, according to this invention it is also possible not to use an epitaxy process on the base layer and, instead, introduce the base profile by implantation before the epitaxial manufacturing of the cap layer.

As illustrated in Figure 9, structured regions consisting of a collector region 112 of the conductivity type II and an insulation region 113 (which surrounds the collector region 112) were produced on a monocrystal substrate layer 111 of the conductivity type I. If the emitter and the collector are, e.g., n-conductive, the base is of the p-type and vice versa. Various suitable insulation techniques are known such as LOCOS processes, spaced mesa arrangements or deep or flat trench insulation.

On the basis of a differential epitaxy process, a buffer layer 114, a SiGe layer with in-situ doping of the base layer 115 of the conductivity type I and a cap layer 116 are is applied on the entire surface.

While the buffer layer 114, the base layer 115 and the cap layer 116 grow – as monocrystal materials – on the silicon substrate, polycrystal layers 114/1, 115/1 and 116/1 arise over the insulation zone 113. After photolithographic masking, dry-etching techniques are applied to remove the epitaxy layer in those regions in which no transistors arise.

If a selective epitaxy process is used instead of differential epitaxy, where growth occurs exclusively on the silicon underground, the structuring of the epitaxy layer stack is eliminated.

In the following step, the silicon regions with an insulation layer 117 are exposed. This can be achieved by means of thermal oxidation and/or deposition. Layer stacks of dielectrica such as silicon oxide and silicon nitride can be applied. Besides that, the electrically conductive layer can be covered with a poly-silicon layer in order to maintain additional flexibility for the process at a later stage.

Essential from the point of view of the procedure according to this invention is the implementation of the cap doping profile in an epitaxially produced cap layer. There is a possibility to introduce similar profiles, as shown in Figure 6, in situ during the epitaxy process. Furthermore, a flat profile can be produced by implantation before or after the production of the insulation layer 117. In addition, various procedures for the diffusion of such profiles are also known. This can also be performed by means of an insulation layer highly enriched with the doping agent. A diffusion step can occur before or after further procedure steps. The use of diffusion-preventing ingredients in the collector, the base and the cap layer 116 such as carbon is especially useful if certain processes are used such as implantation, diffusion or thermal oxidation, which can cause an accelerated diffusion of the doping agents.

The transistor manufacturing process can now proceed with the structuring of a coating mask for the opening of the emitter window. In this step, the cover layers are removed in well-known etching procedures. In order to achieve good transistor properties, preferably wet-etching techniques should be used to expose the semiconductor surface.

The process continues with the deposition of an amorphous silicon layer for the creation of a poly-silicon emitter. This layer can be doped in situ by implantation during or immediately after the deposition.

The process then continues with conventional steps of structuring, implantation and passivation. The required high-temperature steps are taken to cure implantation defects and to form the poly-emitter. The manufacturing process is completed with the opening of the contact apertures for the emitter, the base and the collector and with a standard metallization of the transistor contacts.

This invention explains, on the basis of concrete design examples, a bi-polar transistor and a procedure for its manufacture. However, notice must be taken that this invention is not restricted to the particulars of the description of any particular design example, since, within the patent claims, changes and deviations are also subject to patent protection.

Patent claims

1. A procedure for the manufacture of a bi-polar transistor, during which structured regions consisting of a collector region (112) and an insulation region (113) - which surrounds the collector region (112) - are produced on a monocrystal substrate layer (111), a base layer (115) and, by means of epitaxy, a cap layer (116) are produced over the collector zone (112) – where an interposed buffer layer (114) can be deposited -, an insulation layer (117) is deposited over the cap layer (116), the insulation layer (117) is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer (117) and is then used as an emitter-doping agent source and as a contact layer, **characterized in that** – before the diffusion from the emitter-doping agent source - a doping profile is introduced into the cap layer (116), and the profile is low-doped on the base side and highly doped on the emitter side.

2. A procedure according to claim 1, **characterized in that** the base-side lower doping concentration of the cap layer (116) does not exceed values of 5×10^{16} cm^{-3}.

3. A procedure according to claims 1 or 2, **characterized in that** the cap layer (116) is of a thickness between 20 nm and 70 nm.

4. A procedure according to one or several of the preceding claims, **characterized in that** the emitter-side high doping concentration of the cap layer (116) does not exceed values of 5×10^{18} cm^{-3} if the doping agent is of the same conductivity type as the base layer (115).

5. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced by implantation.

6. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced in situ during the epitaxy process.

7. A procedure according to one or several of the preceding claims, **characterized in that** the cap doping profile is introduced by diffusion from the insulation layer (117) that had been highly enriched with the doping agent.

8. A bi-polar transistor, in which structured regions consisting of a collector region (112) and an insulation region (113) - which surrounds the collector region (112) - are produced on a monocrystal substrate layer (111), a base layer (115) and – where a buffer layer (114) can be interposed -, by means of epitaxy, a cap layer (116) are produced over the collector zone (112), an insulation layer (117) is deposited over the cap layer (116), the insulation layer (117) is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer (117) and is then used as an emitter-doping agent source and as a contact layer, **characterized in that,** in the overlapping region (17) – the region between the edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer (15) – the cap layer

(13/116) contains a doping profile, and the profile is low-doped on the base side and highly doped on the emitter side.

9. A bi-polar transistor according to claim 8, **characterized in that** the base-side lower doping concentration of the cap layer (13/116) does not exceed values of 5×10^{16} cm^{-3}.

10. A bi-polar transistor according to one or several of claims 8 to 9, **characterized in that** the cap layer (13/116) is of a thickness between 20 nm and 70 nm.

11. A bi-polar transistor according to one or several of claims 8 to 10, **characterized in that** the emitter-side high doping concentration of the cap layer (13/116) does not exceed values of 5×10^{18} cm^{-3} if the doping agent is of the same conductivity type as the base layer (12,115).